DIRECT, NON-DESTRUCTIVE MEASUREMENT OF RECESS DEPTH IN A WAFER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an effective, simple, direct and non-destructive method to measure recess depth in a wafer by putting the wafer into a track where a solvent is poured, commencement of spinning the wafer in the track to fill-up the recess, and subsequent spinning-off of the remaining solvent so that no solvent remains on the wafer surface, weighing the wafer, heating to remove the solvent, and again weighing to ascertain the difference in weight or the amount of solvent imbibed by the trenches together with solvent density, to permit a simple calculation of the recess depth.

2. Description of The Prior Art

In the ASG and LOCOS resist or polysilicon recess process, control of the recess depth is crucial as the recess depth determines both parasitic leakage and the capacity of the transistor, thus controlling the storage time of the transistor.

At present, profiling techniques such as those performed with SEMs or AFM are used to monitor the recess depth within round or elliptical depths in a chip.

However, SEM measurements are time-consuming, costly and destructive. On the other hand, AFM measurements of recess depths in a trench is done in the kerf, in which the trench size is large enough to accommodate the bulky AMF tip. Because the recess depth is closely related to the size of the trench, a correlation

needs to be established between the large trench on the kerf and the real trench in the arrays.

U.S. Patent 6,275,297 discloses methods of and apparatus for measuring the depth of structures on a semiconductor substrate. The measurement is accomplished by a broadband light source that irradiates the recessed and non-recessed portions. A detector detects reflected light including a first spectral component comprising light reflected from the recessed portions and a second spectral component comprising light reflected from the non-recessed portions, wherein at least one of the first and second components further comprises a third component comprising light reflected from the dielectric layer. Spectral reflectance information of the detected rays is stored and a plot of reflectance intensity versus wavelength is generated. Depth geometries of the recesses and the dielectric layer are determined relative to the at least one reference interface based on an interferometric analysis of the plot.

An assembly for measuring a trench depth parameter in a work-piece is disclosed in U.S. Patent No. 5,691,540. The assembly comprises an ultra-violet radiation source; a split fiber bundle having a first branch for propagating the ultra-violet radiation from the radiation source to a lens, and a second branch; a lens for focusing the UV radiation to the workpiece and refocusing an ultra-violet interference signal to the second branch; and a detector responsive to the ultra-violet interference signal received through the second branch. The detector transforms the ultra-violet interference signal to an electrical signal which is a measure of a trench depth of the workpiece. The ultra-violet interference signal is developed when ultra-violet radiation propagates through the workpiece and reflects from its base region to thereby interfere with ultra-

violet radiation that is directly reflected by a workpiece surface which is different from the base region.

U.S. Patent 6,124,141 discloses a non-destructive method for measuring the depth at which the top surface of a buried interface is located in a semiconductor substrate. The method employs a Fourier Transform Infrared measurement, and comprises subjecting the semiconductor substrate containing the buried interface to a beam of infrared light and then detecting and analyzing the spectrum of a return signal by a Fourier analysis. The spectrum as analyzed by the Fourier analysis is then compared to calibration spectra to thereby determine the depth of the top surface of the buried interface. The invention also uses a device for determining the depth of a buried interface below the surface of a semiconductor substrate. That device comprises a FTIR spectrophotometer which illuminates the substrate with a source of infrared radiation and which produces a Fourier transform of a return signal reflected from the substrate. The device includes a library of stored calibration spectra, along with means for comparing the Fourier transform return signal to the calibration spectra to determine the depth of the buried interface.

U.S. Patent 4,840,487 discloses an apparatus for measuring etching pits by employing a light source having a small absorptivity with respect to a groove or pit as an object of irradiation to insure a satisfactory change in the interference intensity of the defracted light which is reflected from the object. The apparatus includes a detector means provided with the freedom of movement in two axial directions which are perpendicular to each other and in the direction of rotation. In addition, as a laser source, a He-Cd, N_2 or Ar laser may be employed in addition to a He-Ne laser to detect changes in their interference intensities, and the etch depth is calculated on the basis of the detected changes.

There is a need in the art of measuring recess depth in the wafer for an effective, simple, direct and non-destructive measurement technique for recess process control, especially with device dimensions of groundrule shrinkage to 0.13 microns and below, as the current profiling techniques are becoming increasingly more costly and difficult to correlate.

SUMMARY OF THE INVENTION

One object of the present invention is to provide an effective and non-destructive measurement technique for recess process control or depth measurement in a semiconductor chip, where the device dimensions or ground rules have shrunk to 0.13 microns and below.

Another object of the present invention is to provide a simple, non-destructive measurement technique for recess process control or depth where the device dimension or groundrules have shrunk to 0.13 microns and below without employing SEM or AMF profiling techniques.

A further object of the present invention is to provide a direct, non-destructive measurement technique for recess process control or depth measurement in a semiconductor, where device dimension or ground rules have shrunk to 0.13 microns and below, that are less costly and less difficult to correlate.

In general, the effective, simple, direct and non-destructive method for measuring recess depth in a semiconductor chip of the invention is through the use of a solvent, and entails:

placing the recessed wafer into a track where a solvent is poured onto the wafer and commencing spinning of the wafer to recess the solvent into the trench and fill it up;

subsequently spinning off the remaining solvent so that no solvent remains on the surface of the wafer;

weighing the wafer;

heating to remove the solvent;

again weighing to ascertain the difference in the two weights or the amount of the solvent imbibed by the trenches; and

calculating recess depth premised around the density of the solvent and the weight difference.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a Scanning Electron Micrograph of a typical wafer profile after resist recess and etching.

FIG. 2 is a schematic of the non-destructive method of measuring recess depth of a wafer utilizing a solvent in accordance with the invention process.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT OF THE INVENTION

Reference is now made to FIG. 1 which shows scanning electron micrographs (SEMs) of a typical wafer profile after resist recess and etching. The recess material Accuflow 913 EL from Honeywell. The POR resist recess etch recipe was applied to the wafer. From x-section pictures of the array center, and array edge, the most important data is collected; namely, the recess depth. In addition to the recess depth, information regarding the maximum variation is also collected, that is, the maximum variation within the wafer is 0.22 microns, within the array centers 0.11 micron and from the array center to the edge 0.14 microns or smaller.

For a 110nm DRAM product, there is a 308 chips per 8 inches of wafer, and a half billion trenches per chip. Assuming that each trench has a width of 1.25nm, a length of 220 nm, and a depth of 1.3 microns, the total volume of trench that would have potential to be filled by a solvent is approximately 4.3mm^3 . The particular solvent utilized has a density or specific gravity of about 1.4g/cm^3 , and the weight difference is about 6mg. The balance scale utilized is easily capable of weighing up to 100g with a resolution of up to 0.05mg. This corresponds to less than 1% noise level; in other words, easy measurement of a trench with recess depth of 1.3 microns can be made with an accuracy of up to 13nm.

FIG. 2 is a schematic of the invention process for measuring the recess depth of a semiconductor chip. After recess, the wafers are put into a track where several mil of a solvent with a density of 1.4g/cm3 is poured into the wafers, whereupon spinning is started. Because of the capillary force between the surface of the trenches and the solvent, the solvent easily recesses into the trench and fills it up. A subsequent spinning step is used to spin off the remaining solvent and render a wafer with trench filled with the solvent. However, at this juncture no solvent remains on the surface of the wafer. The wafer is weighted by a balance and then placed into a hot plate to remove the solvent by evaporation, whereupon the wafer is weighed again. The difference of the weight is the weight of the solvent imbibed by the trenches.

FIGS 2a to 2b depicts a wafer after it is put into a track and solvent is first applied, followed by commencement of spinning.

FIG. 2c depicts the wafer filled with the solvent.

FIG. 2d depicts the wafer after the second spinning process.

FIG. 2e depicts the wafer after it is put into a balance and weighted following removal of the solvent by heating to obtain weight W2.

The following calculations will show the amount the solvent that can be imbibed by 8 inches of wafer in the invention process:

The volume of one DT trench is

$$1.3\text{um} * \text{Pi} * 125/2\text{nm} * 220/2\text{ nm} = 2.8\ 10^{-11}\text{mm}^3$$

The number of DT per wafer is $308 \times 0.5 \times 10^9 = 1.54 \times 10^{11}$

The total volume of DT trenches per wafer is $2.8 \times 10^{-11}\ \text{mm}^3 \times 1.54 \times 10^{11} = 4.3\ \text{mm}^3$

Assume the density of solvent is 1.4g/cm^3, the weight of the solvent that can be imbibed by trenches = $4.3\ \text{mm}^3 \times 1.4\text{g/cm}^3$ = 6.0mg

The balance used can easily measure a 100g object with resolution up to 0.05mg.

The invention method takes advantage of capillary force between the surface of the trenches and the chosen solvent. Capillary force is the reaction between contacting surfaces of a liquid and a solid that distorts the liquid surface from a planar shape; it works very effectively in the size range of 1-100 microns.

The invention method is not limited to 110nm DRAM products or recess processes. The method is applicable to any process wherein there is a need to monitor the depth of huge numbers of trenches with relatively uniform depth across the wafers.